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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MENGISTU, AMARE	
ART UNIT	**PAPER NUMBER**
2673	

DATE MAILED: 03/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/924,973	RAST, RODGER H.	
	Examiner	Art Unit	
	Amare Mengistu	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16-26,47-73 and 77-85* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-26,47-73 and 77-85* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 17,21,22,25,26,55,63-68,71,78,79-80,82-85 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The specification as first filed does not disclose the following claims limitations:

The recitation of claim 17, " ***wherein said input comprises a single line coupled directly to each said display element within a given display array, or signal superimposed on the power being supplied to each said display element within said display array";***

The limitation of claim 21 "***wherein said input comprises a separate signal connection aside from the power and ground connection of said display element***";

The recitation of claim 22 " ***wherein said input is received as a signal superimposed over said power and ground connections to said display element***";

The recitation of claim 25, "***wherein said driver circuit is configured form modulating the optical state of each of said optical elements to either an on or off state in response to said data from said latch circuit***";

The claim limitation of 26 "***wherein said driver circuit is configured from modulating the optical state of each of said optical elements to a desired intensity, color or combination of intensity and color, in response to said data from said latch circuit***";

The limitation of claim 54 ***"wherein said data comprises either a single line coupled directly to each said display element within a given array of said display elements, or is superimposed on the power being supplied to each said display element within the array of display elements";***

The recitation of claim 55 ***"means for modulating the output of the optical state of said at least one optical element is configured to update the optical state of said optical element at a fixed position within cycles of said data signal***";

The claim limitation of 63 "***programming means is configured for loading said address form the data signal in response to a programming signal received by said display element and not by other display elements within an array which are not respond to given said second address***";

Claim 64 recitation ***"said programming means is configured to program said second address in response to a combination of data received from said data signal and said programming signal***";

The recitation of claim 65 "***an optical detector within said display element, said optical detector configured for receiving said programming signal***"

The limitation of claim 66 ***"wherein said optical detector comprises one or more of said at least one optical elements which are configured from both display optical state and detecting optical input"***;

The claim limitation of 67 "***wherein said optical detector comprises at least one separate optical input sensor integrated within said display element***";

The recitation of claim 68 "***wherein said output control data is received on the data signal in a sequential scan form or random form***";

The claim limitation of 71" ***said outputting means is configured for programming said second address within said means with the display element connected in situ on the target array"***;

The claim limitation of 79 '***wherein said programming operation is performed in response to receiving an external optical programming signal while said display element is in a programming mode which loads an address received the display element, in parallel with other display elements within an array of said display elements***";

The recitation of claim 80 "***wherein said external optical programming signal configured for establishing an array position address into each of the display elements contained within an array of display elements***";

The claim 82 limitation "***wherein said driver circuit is configured for providing analog or digital intensity control";***

The recitation of claim 83 "***wherein said memory, said extracting means and said modulating means are incorporated within the die of an optical element, or on an integrated circuit die to which one or more optical elements are bonded***" and,

The claim limitation of 84 "***wherein said memory, said extracting means and said modulating means are intergrated with a red, green and blue optical element retained in said optical housing".***

The recitation of claim 85 "***an optical detector within said display element, said optical detector configured for receiving said program signal, wherein said optical detector comprises one or more of said at least one optical elements which are configured for both displaying optical states and detecting optical input"; and, "wherein said optical detector comprises at least one separate optical input sensor integrated within said display element***".

Thus, applicant's specification fails to enable one of the ordinary skill in the art at the time of the filing to practice applicants claimed invention.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 18 and 84 recites the limitation **"said data load signal"**, **"said optical housing"** in line 4-5. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 47 and 70 are rejected under 35 U.S.C. 102(b) as being anticipated by **Kitada (5,995,070).**

As to claim 47, **Kitada** discloses a display element having internal control circuitry comprising: at leas one optical element intergrated within a display element configured for displaying multiple optical states (fig.7 (2), (8x8 DOT MATRIX LED DISPLAY DEVICE),it is inherent to have multiple optical state, such as ON and OFF); a memory configured for programming to a first address associated with the position of said display elements within an array of said display elements (see, fig. 7 (4), col.9, lines 31-47); means for extracting output data from a data signal, received in parallel by the display element and other display elements with an array of display elements, in response to matching a second address received on said data signal with said first address (see. Fig 7 (9), col.9, lines 31-47, col. 12, lines 46-65); means for modulating the output of

said at least one optical element in response to said extracted output data (see.fig.7 (10), col.17, lines 35-61)).

In regard to claim 70, **Kitada** also discloses a display element having internal control circuitry comprising: at least one optical element integrated within a display element configured for displaying multiple optical state (fig.7 (2), (8x8 DOT MATRIX LED DISPLAY DEVICE), it is inherent to have multiple optical state, such as ON and OFF); means for outputting optical state data, received from a data signal common to all display elements in the array, to said at least one optical element in response to matching a first address received (fig.7 (9)) from the data signal with a second address programmed within said means to the position of the display element within an array of the display elements (see, col.4 lines 46-67, col.9, lines 19-47. Here note, "second address" is interpreated as update address).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 16 and 61 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kirada (5,995,070)** in view of **Takahashi (5,233,337).**

As to claims 16 and 61, **Kirada** discloses a display element having internal optical control circuit comprising: at least one optical element integrated within a display element configured for displaying multiple optical states (see. Fig.7 (2) (8x8 dot matrix LED display), it is inherent for LED to have multiple optical states (ON/OFF states)); an input configured for receiving an array position addressing signal containing array position clocking and data which are delivered in common to all said display elements within a single or multidimensional display array (see, fig.7 (2,6), col.12, lines 25-27); a counter configured for maintaining an array position count in response to detecting said array position clocking form said input (fig.7 (8)); a memory configured for retaining an array position (see, fig.7 (4)); a comparison circuit configured for generating a data load signal in response to detecting a desired relationship between said array position maintained by said counter and said array position retained in said memory (see, fig.7 (9)) and a driver circuit configured for outputting said data to update the optical state of said at least one optical elements (see, fig.7 (11-13)).

Kirada has failed to teach a latch circuit. However, **Takahashi** clearly teaches that it is well known for LED to have a latch circuit configured for loading data from said input in response to receipt of said data load signal (see figs. 4 and 7(62)).

Therefore, it would have been obvious to one skill in the art at the time of the invention was made to have been motivated to incorporate the latch circuit of **Takahashi** into the LED display system of **Kirada** because this will help to hold the data in a circuit until other circuits are ready to change the latch circuit.

As to claims 17 and 54, **Takahashi** discloses a single signal line coupled directly to each said display element within a given display array (see, figs. 4 and 7 (24,68)).

As to claim 18, also teaches a shift register coupled to an input. and said shift register is configured to output in parallel the data bits it has received to said latch (see, figs.4 and 7 (60)).

As to claim 19, **Kirada** disclose a memory (fig.7 (4)). It is well known for a memory to have a non-volatile memory.

As to claim 20, **Kirada** also discloses said memory is configured for being loaded with an array position value in response to a position programming operation (see, fig. 7(6), col.10, lines 19-32).

As to claim 23, **Kirada** discloses said array position clocking and data are received for each array address in each cycle of an array position addressing signal (see, fig. 7 (10,12)).

In regard to claim 24, **Kirada** teaches said driver is configured for outputting said data to said at least one optical element in response to detecting the end of said cycle of said array position addressing signal (col.9, lines 19-30).

As to claim 48 **Takahashi** states that said first address comprises at least one axis of addressing (figs. 4 and 7(68)).

In regard to claim 49, **Kirada** discloses that said first address comprises at least one axis of addressing (see, fig. 7(2)).

As to claim 50, **Kirada** suggest that said means for extracting data is configured for extracting a predetermined number of data bits for said data signal (see, col.8, lines 36-52, col.14, lines 4-19).

In regard to claim 51, **Kirada** also discloses means for extracting data is configured for counting clocks on said data signal for determining said second address (see, col.12, lines 46-57).

As to claim 52, **Kirada** discloses that said clocks comprise column and row clocks (see, col.9, lines 6-10, 48-63).

As to claim 53, **Kirada** also teaches that means for extracting data is configured to detecting a rest clock to reset the clocks being counted in determining said second address (see, col.9, lines 6-10, col.12, lines 46-54).

In regared to claim 55, **Kirada** also teaches said means for modulating the output of the optical state of said at least one optical element is configured to update the optical state of said optical element at a fixed position within cycles of said data signal (col.10, lines 66- col.11, lines 15).

As to claim 56, **Kirada** discloses said fixed position occurs at the end of a cycle of said data signal (see, fig.10).

In regard to claim 57, **Kirada** also discloses said means for extracting comprises: a counter configured for counting clocks to determine said second address within said data signal (see, fig.7 (8),col.9, lines 6-9); an address comparator for generating a matching signal in response to detecting a predetermined relationship between said second address determined by said counter and said first address retained within said

memory (see, fig.7 (9), col.9, lines 10-47). **Takahashi** teaches that the data store configured for collecting data bits from said data signal (see, fig.4 (60,62)) and **Kirada** discloses a matching signal (fig.7 (9)).

As to claims 58-60 **Kirada** also teaches said modulating means comprises: a driver ciruict configured for driving said at least one optical element to provide intensity, color or combination of intensity and color (figs.7 (11-13) and 6A , col.8, lines 7-26) and **Takahashi** teaches a latch configured for latching and outputting data from stored (fig.4 (62),(60)).

As to claim 62, **Kirada** further teaches that means for programming said memory to said first address in response to the position of the display element with an array of the display element (see, col.4, lines 46-53).

In regard to claim 63, **Kirada** discloses said programming means is configured for loading said address form the data signal in response to a programming signal received by said display element and not by other display elements within an array which are not respond to given said second address (see, col.4, lines 53-67).

As to claim 64, **Kirada** teaches said programming means is configured to program said second address in response to a combination of data received from said data signal and said programming signal (see, col.4, lines 53-67).

As to claim 68, **Kirada** also teaches that said output control data is received on the data signal in a sequential scan form or random scan form (see, figs. 10 and 12). It is also well known in a display art to use a sequential scan form or random scan form.

As to claim 71, **Kirada** also discloses said outputting means is configured for programming said second address within said means with the display element connected in situ on the target array (see, col.10, lines 19-32).

In regard to claim 72, **Kirada** further teaches that said outputting means is configured for receiving said data signal which each display element monitors within the array of display elements (see, col.10, lines 1-15).

As to claims 73 and 81, **Kirada** as modified by **Takahashi** suggests that said second address is programmed (see, col.4, lines 46-67,col.8, lines 36-52 of **Kirada**) and onto memory within said outputting means (see, **Takahashi** fig.4 (60)). As to the memory being non-volatile is well known.

In regard to claim 77, **Kirada** does not teach that the display element is contained within an optical housing configured with a transparent portion through which the state of said at least one optical element can be viewed. However, it is obvious for LED display device to have a housing in order to protect the LED from damage.

As to claim 78, **Kirada** disclose said memory configured for storing said first address for the display element in response to a programming operation that programs the position of said display element according to its position within an array of display elements (see, col.9, lines 31-47).

Response to Arguments

9. Applicant's arguments with respect to claims 16-26,47-73,77-85 have been considered but are moot in view of the new ground(s) of rejection.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Amare Mengistu whose telephone number is (571) 272-7674. The examiner can normally be reached on M-F,T-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3639. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Amare Mengistu
Primary Examiner
Art Unit 2673

AM

March 9,2006